IN THE CLAIMS

1. (Original) A process of treating a semiconductor structure comprising:

providing a substrate;

providing a gate stack comprising a gate dielectric layer disposed over the substrate; a polysilicon layer disposed over the gate dielectric layer; a barrier layer disposed over the gate dielectric layer, and a metal film disposed over the polysilicon layer; and

oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film.

2. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using a fluorine-containing composition disposed in a layer over the gate stack.

3. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using fluorine disposed in a dielectric cap layer over the metal film.

4. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using fluorine disposed in a dielectric cap layer disposed over the metal film, wherein the dielectric cap layer contains fluorine in a range from about 0. 1% to about 30%.

5. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using a fluorine-containing composition that is metered to the substrate and gate stack in gaseous form.

6. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include usingNF3 gas that is metered to the substrate and gate stack.

7. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using a fluorine-containing composition disposed in a layer in the gate

stack, and a fluorine-containing composition that is metered to the substrate and gate stack in gaseous form.

8. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using fluorine disposed in a dielectric nitride cap layer over the metal film, wherein the dielectric nitride cap layer contains fluorine in a range from about 0.1% to about 30%.

9. (Original) A process comprising:

forming a metal film over a structure; and

thermally processing the structure in the presence of a first composition such that the metal is more likely to combine with at least a portion of the first composition than with the structure.

10. (Original) The process according to claim 9, wherein the structure comprises oxide surfaces, and wherein the conditions are sufficient to cause the first composition to resist etching the oxide surfaces.

11. (Original) The process according to claim 9, wherein the first composition comprises NF3.

12. (Original) The process according to claim 9, wherein the first composition comprises NF3 in a gaseous state.

13. (Original) The process according to claim 9, wherein the first composition comprises NF3 in a solid state.

14. (Original) The process according to claim 9, wherein the first composition comprises a halogen-containing composition.

15. (Original) The process according to claim 9, wherein the first composition comprises a halogen-containing composition in a gaseous state.

16. (Original) The process according to claim 9, wherein the first composition comprises a halogen-containing composition in a solid state.

17. (Currently Amended) The process according to claim 9, further comprising:

forming a spacer layer over the structure; and

~~spacer~~ etching the spacer layer.

18. (Original) A process comprising:

forming a doped polysilicon layer over a substrate;

forming a barrier layer over the doped polysilicon layer;

forming a metal film over the metal nitride barrier layer;

forming a nitride layer over the metal film to form a gate stack disposed on a substrate; and

thermally processing the gate stack in the presence of a fluorine-containing composition under conditions sufficient to cause the metal film more likely to combine with the fluorine-containing composition than with the gate stack or the substrate.

19. (Original) The process according to claim 18, wherein the barrier layer includes a metal nitride barrier layer.

20. (Original) The process according to claim 18, wherein the gate stack and the substrate include oxide surfaces, and wherein the conditions are sufficient to cause the fluorine-containing composition to resist etching the oxide surfaces.

21. (Original) The process according to claim 18, wherein the fluorine-containing composition comprises NF3.

22. (Original) The process according to claim 18, wherein the metal film is selected from Al, Cu, Ag, Au, Ti, Zr, Hf, Ni, Co, Pd, Pt, V, Ta, Nb, Cr, Mo, W, Sc, Yt, La, Ce, Rh, Os, Ir, and combinations thereof.

23. (Original) The process according to claim 18, wherein the fluorine-containing composition comprises NF3 in a solid state.

24. (Original) The process according to claim 18, wherein the fluorine-containing composition comprises the nitride layer.

25. (Original) The process according to claim 18, wherein the fluorine-containing composition comprises the metal film.

26. (Original) The process according to claim 18, wherein the fluorine-containing composition comprises the metal nitride barrier layer.

27. (Original) A process of forming a gate stack comprising:

providing a substrate;

forming a gate dielectric layer over the substrate;

depositing a polysilicon layer over the gate dielectric layer;

forming a metal film above the polysilicon layer;

forming a cap layer over metal film;

etching a gate stack through the cap layer, the metal film, and the polysilicon layer, under conditions that reduce redeposition on the substrate of a volatilized portion of the metal film; and

wherein at least one process of depositing a polysilicon layer, forming a metal film, and forming a cap layer is carried out in the presence of a metal-reducing composition.

28. (Original) The process according to claim 27, wherein the conditions that reduce redeposition include using a halogen-containing composition that is metered to the substrate in gaseous form.

29. (Original) The process according to claim 27, wherein the conditions that reduce redeposition include using NF3 gas that is metered to the substrate.

30. (Original) The process according to claim 27 following etching a gate stack, further comprising:

oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film.

31. (Original) The process according to claim 27 following etching a gate stack, further comprising:

oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film; and

forming a spacer layer over the gate stack under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film.

32. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using a halogen-containing composition that is metered to the substrate and gate stack in gaseous form.

33. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using NF3 gas that is metered to the substrate and gate stack.

34. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using a halogen-containing composition disposed in a layer or the film in

the gate stack, and a halogen-containing composition that is metered to the substrate and gate stack in gaseous form.

35. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using fluorine disposed in the cap layer over the metal film.

36. (Original) A process of making a computer system, comprising:

forming a processor;

forming a memory system coupled to the processor; and

forming an input/output circuit coupled to the processor and the memory system; wherein at least one of forming a processor and forming an input/output circuit include:

providing a substrate;

forming a gate dielectric layer over the substrate;

depositing a polysilicon layer over the gate dielectric layer;

forming a metal film above the polysilicon layer;

forming a cap layer over metal film;

etching a gate stack through the cap layer, the metal film, and the polysilicon layer, under conditions that reduce redeposition on the substrate of a volatilized portion of the metal film; and

wherein at least one process of depositing a polysilicon layer, forming a metal film, and forming a cap layer is carried out in the presence of a metal-reducing composition.

37. (Original) The process according to claim 36, wherein the memory system is disposed in a host selected from a memory module, a device driver, a power module, a communication modem, a processor module, and an application specific integrated circuit.

38. (Withdrawn) A system comprising:

a semiconductor structure comprising a substrate;

a metal film disposed over the substrate;

wherein the metal film is selected from Al, Cu, Ag, Au, Ti, Zr, Hf, Ni, Co, Pd, Pt, V, Ta, Nb, Cr, Mo, W, Sc, Yt, La, Ce, Rh, Os, Ir, and combinations thereof;

a processing tool comprising a chamber; and

at least one getterer composition selected from a getterer gas and a getterer solid, wherein the at least one getterer composition comprises a thermodynamic or kinetic advantage over the semiconductor structure for combining with the metal film.

39. (Withdrawn) The system according to claim 38, wherein the getterer solid comprises a dielectric layer disposed over the semiconductor structure.

40. (Withdrawn) The system according to claim 38, wherein the getterer solid comprises a metal film disposed over the semiconductor structure.

41. (Withdrawn) The system according to claim 38, wherein the getterer solid comprises a dielectric layer or metal film disposed over the semiconductor structure, wherein the dielectric layer or metal film comprises from about 1% fluorine to about 30% fluorine.

42. (Withdrawn) The system according to claim 38, wherein the getterer solid comprises a conductive nitride layer disposed over the semiconductor structure, wherein the conductive nitride layer comprises from about 0.1% fluorine to about 30% fluorine.

43. (Withdrawn) The system according to claim 38, wherein the getterer gas comprises a fluorine-containing composition.

44. (Withdrawn) The system according to claim 38, wherein the getterer gas comprises a fluorine-containing composition in a volumetric concentration range from about 0.1% to about 10%.

45. (Withdrawn) The system according to claim 38, wherein the getterer gas comprises NF3 in a volumetric concentration range from about 0.1% to about 10%.

46. (Withdrawn) The system according to claim 38, wherein the getterer gas comprises a halogen selected from F, Cl, Br, I, and combinations thereof.

47. (Withdrawn) A system comprising:

a gate dielectric layer disposed over a semiconductor substrate;

a doped polysilicon electrode disposed over the gate dielectric layer;

a tungsten nitride barrier layer disposed over the polysilicon electrode;

a metal film disposed over the tungsten nitride barrier layer, wherein the metal film is selected from Al, Cu, Ag, Au, Ti, Zr, Hf, Ni, Co, Pd, Pt, V, Ta, Nb, Cr, Mo, W, Sc, Yt, La, Ce, Rh, Os, Ir, and combinations thereof;

a processing tool comprising at least one chamber; and

at least one composition selected from a gas and a solid, wherein the at least one composition comprises a thermodynamic or kinetic advantage over the semiconductor substrate for combining with metal from the metal film.

48. (Withdrawn) The system according to claim 47, wherein the solid comprises a dielectric film disposed over the metal electrode.

49. (Withdrawn) The system according to claim 47, wherein the solid comprises a dielectric film disposed over the semiconductor structure, wherein the dielectric film comprises from about 0.1% fluorine to about 30% fluorine.

50. (Withdrawn) The system according to claim 47, wherein the solid comprises a nitride dielectric film disposed over the semiconductor structure, wherein the nitride dielectric film comprises from about 0.1% fluorine to about 30% fluorine.

51. (Withdrawn) The system according to claim 47, wherein the gas comprises a fluorine-containing composition.

52. (Withdrawn) The system according to claim 47, wherein the gas comprises a fluorine-containing composition in a volumetric concentration range from about 0.1% to about 10%.

53. (Withdrawn) The system according to claim 47, wherein the gas comprises NF3 in a volumetric concentration range from about 0.1% to about 10%.

54. (Withdrawn) The system according to claim 47, wherein the solid comprises a nitride dielectric film disposed over the semiconductor structure, wherein the nitride dielectric film comprises from about 0.1% fluorine to about 30% fluorine; and wherein the gas comprises NF3 in a concentration range from about 0.1% to about 10%.

55. (Withdrawn) A gate stack comprising:

a substrate;

a gate dielectric layer disposed above and on the substrate;

a doped polysilicon layer disposed over the gate dielectric layer;

a conductive barrier layer disposed over the polysilicon layer;

a metal film disposed over the conductive barrier layer;

a dielectric cap layer disposed over the metal film; and

wherein at least one of the conductive barrier layer, the metal film, and the dielectric cap layer include a halogen disposed therein in a range from about 0.1% to about 30%.

56. (Withdrawn) The gate stack according to claim 55, wherein the halogen includes fluorine.

57. (Withdrawn) The gate stack according to claim 55, wherein the conductive barrier layer, the metal film, and the dielectric cap layer each include a halogen disposed therein in a range

from about 0.1% to about 30%.

58. (Withdrawn) The gate stack according to claim 57, wherein the halogen includes fluorine.

59. (Withdrawn) The gate stack according to claim 55, wherein for the conductive barrier layer, the metal film, and the dielectric cap layer only two thereof include a halogen disposed therein in a range from about 0.1% to about 30%.

60. (Withdrawn) The gate stack according to claim 59, wherein the halogen includes fluorine.

61. (Withdrawn) The gate stack according to claim 55, wherein for the conductive barrier layer, the metal film, and the dielectric cap layer only one thereof comprises a halogen disposed therein in a range from about 0.1% to about 30%.

62. (Withdrawn) The gate stack according to claim 61, wherein the halogen comprises fluorine.

63. (Withdrawn) A computer system, comprising:

a processor;

a memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the memory system; and

a gate stack disposed in at least one of the processor and the I/O circuit, the gate stack including:

a substrate;

a gate dielectric layer disposed above and on the substrate;

a doped polysilicon layer disposed over the gate dielectric layer;

a conductive barrier layer disposed over the polysilicon layer;

a metal film disposed over the conductive barrier layer;

a dielectric cap layer disposed over the metal film; and

wherein at least one of the conductive barrier layer, the metal film, and the dielectric cap layer include a halogen disposed therein in a range from about 0.1% to about 30%.

64. (Withdrawn) The computer system according to claim 63, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, and an aircraft.

65. (Withdrawn) A system, comprising:

a circuit module having a chip set; and

a gate stack disposed in at least one of the chips in the chip set, the gate stack including:

a substrate;

a gate dielectric layer disposed above and on the substrate;

a doped polysilicon layer disposed over the gate dielectric layer;

a conductive barrier layer disposed over the polysilicon layer;

a metal film disposed over the conductive barrier layer;

a dielectric cap layer disposed over the metal film; and

wherein at least one of the conductive barrier layer, the metal film, and the dielectric cap layer include a halogen disposed therein in a range from about 0.1% to about 30%.

66. (Withdrawn) The system according to claim 65, wherein the circuit module is disposed in a host selected from a memory module, a device driver, a power module, a communication modem, a processor module, and an application specific integrated circuit.

Claim 17 is amended, claims 38-66 remain withdrawn. Claims 1-66 are pending.

The Examiner is invited to contact Applicant's Representatives at the below-listed telephone number if there are any questions regarding this Response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

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